REMARKS

Claims 1-14 are pending in this application of which claims 1 and 7 are independent. Claims 6 and 12 have been withdrawn from consideration. For the following reasons, this application should be considered in a condition for allowance and passed to issue.

Claim objections

The Examiner objects to claim 7 and suggests that the term "correcting means" should be --calibration means--. Claim 7 has been amended to recite "calibration circuitry." Withdrawal of the objection is respectfully solicited.

Claim rejections - 35 U.S.C. § 112

The Examiner rejects claims 1-5, 7-11 and 13-14 under 35 U.S.C. § 112, second paragraph, as being indefinite. The rejection is respectfully traversed.

Regarding claim 1, the Examiner states that "it is unclear who/what generates a trigger signal? and who/what reads the stored data?" Also, regarding claim 3, the Examiner states "it is unclear what/how calibration data file is created?" To the contrary, the claims at issue recite a semiconductor integrated testing method comprising various steps, yet the Examiner seems to assert that the claims are indefinite as the steps of the claims do not recite structure. That is, in order to satisfy the questions of who/what performs an operation or how a particular file is created, the steps of the claims would need to incorporate structure. However, there is no legal requirement per se that structure must be incorporated into a method claim. The second paragraph of 35 U.S.C.§ 112 requires that a claim particularly point out and distinctly claim what applicant considers to be the

invention. The invention claimed is a method with each step particularly and distinctly pointed out.

Regarding claim 4, the Examiner states that "it is not clear what is functional test?" To the contrary, there is no ambiguity in the phrase "functional test performed by said tester," as this phrase is clearly defined in the specification. Claim 4 has been amended to correct an apparent antecedent basis problem. The term "functional test" has been replaced with --a functional test--.

Regarding claim 7, the Examiner states that "it is not clear what is 'input waveform timing'?" The Examiner also questions who measures that measuring signal and how the device is related to the correcting means. In order to respond, claim 7 has been amended to recite "calibration circuitry for determining waveform timing delay from said wiring lengths based on iterative measurements in time of the measuring signal by said semiconductor integrated circuit under test at each pin." The claim language now particularly points out that the semiconductor integrated circuit under test measures the measuring signal in time in order to determine waveform timing delay from the wiring lengths. Accordingly, it is submitted that the rejection has been overcome.

Finally, the Examiner indicates that all claims that depend from the rejected claims are also rejected. It is believed that all issues have been addressed, and corrected when necessary. Withdrawal of the rejection is respectfully solicited.

Claim rejections - 35 U.S.C. § 102

The Examiner rejects claims 1-5, 7-9, 11 and 13-14 under 35 U.S.C. § 102(b) as being anticipated by Otsuji et al. (hereinafter "Otsuji") (U.S. Patent No. 4,928,278). The rejection is respectfully traversed.

Otsuji discloses an integrated testing system for calibrating timing errors at each pin of an IC under test. The system incorporates pin electronic units 9-1...9-n externally connected to the input/output pins of the IC device 1 under test. In order to calibrate timing errors to the IC under test, a reference timing signal 11 is supplied to all pins of the IC under test and to a comparator 5 located on each pin electronic unit. Output signals at each pin of the IC under test are supplied to the comparator and compared against the reference timing signal. Depending on the number of "n" times that the comparison result is judged to be high or low, timing errors may be determined for each pin of the IC under test.

Claim 1 has been amended to recite a semiconductor integrated circuit testing method in which the latching step is performed by the actual semiconductor integrated circuit under test. Moreover, the storage step stores the latched memory signal into the storing means, which is incorporated into the semiconductor device under test. Also, claim 7 now recites "calibration circuitry for determining waveform timing delay from said wiring lengths based on iterative measurements in time of the measuring signal by said semiconductor integrated circuit under test at each pin." In other words, iterative measurements of the measuring signal are performed by the semiconductor integrated circuit under test at each pin.

In comparison to Otsuji, the testing and measurement circuitry is incorporated in pin electronic units, which are not part of the IC under test. To put it another way, Otsuji fails to disclose or suggest "latching said memory signal by said semiconductor integrated circuit under test by use of said triggering signal" and "storing the latched measuring signal as data into storing the means incorporated in said semiconductor circuit under test."

Otsuji also fails to disclose or suggest "calibration circuitry for determining waveform timing delay from said wire lengths based on iterative measurements in time of the measuring signal by said semiconductor integrated circuit under test at each pin."

Claims 1 and 7 are patentable for the foregoing reasons. Claims dependent therefrom are patentable based at least on their dependency and for novel features recited therein. Withdrawal of the anticipation rejection is respectfully solicited.

Claim rejections - 35 U.S.C. § 103(a)

The Examiner rejects claim 10 under 35 U.S.C. § 103(a) as being unpatentable over Otsuji "as applied to claims 8 and 7 above." This rejection is respectfully traversed.

While claim 10 is patentable at least based on its dependency from allowable claim 7, the Examiner's further analysis is flawed. For example, the Examiner acknowledges that Otsuji does not disclose FIFO memories and scan FF circuits. The Examiner states that it would have been obvious to one of ordinary skill in the art at the time invention to use FIFO memories and scan FF circuits. The Examiner alleges that it is well known in the art that memories and scan circuits are used to temporarily store data, as evidenced by U.S. Patent No. 4,688,211 ("the '211 patent"). The Office Action does not provide a copy of this reference nor does it cite this patent in a PTO 892 Form. Nevertheless, the '211 patent relates to a telecommunication switching system for providing high reliability between and through the use of two interface circuits, and is thus directed to a different field of endeavor.

The Office Action presents no rationale as to why a person or ordinary skill in the art of memory testing would have found the telecommunication teachings of the '211 patent pertinent to Otsuji.

The requisite motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. § 103 is not an abstract concept, but must stem from the applied prior art as a whole and have realistically impelled one of ordinary skill in the art to modify a specific reference or combine specific references to arrive at a claimed invention. In this case, the Examiner attempts to incorporate a teaching from a wholly separate field of endeavor, telecommunication switching systems, so as to support a conclusion of obviousness. The Examiner has not met the burden of establishing obviousness. Withdrawal of the obviousness rejection is respectfully solicited.

Conclusion

If there are any questions regarding this response or the application in general, a telephone call to the undersigned would be appreciated in order to expedite prosecution of this case.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

David M. Tennant
Registration No. 48,362

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 SAB:DT:lf
Facsimile: (202) 756-8087
Date: July 3, 2003